What is claimed is:

1. A multiple arbitration circuit capable of simultaneously arbitrating multiple paths from *n* source ports to *n* destination ports at the same instance in time.

2. The circuit according to claim 1 wherein *n* represents the maximum number of ports on said corsspoint switched bus.

3. The circuit according to claim 2 further comprising a multiple arbitration unit connected to the crosspoint switched bus.

4. The circuit according to claim 3 wherein said multiple arbitration unit includes a request decoder for decoding a requested destination port.

5. The circuit according to claim 3 wherein said multiple arbitration unit includes a prioritizer for determining a destination address for each piece of data entering the circuit and then prioritizing data for each requested destination based on preprogrammed priority ranking.

6. The circuit according to claim 5 wherein said multiple arbitration unit includes a crosspoint select encoder for decoding the output of the prioritizer and for encoding a crosspoint select value for said crosspoint switched bus.

7. The circuit according to claim 3 wherein said multiple arbitration unit includes an acknowledge OR for gathering acknowledges from said source ports and logically arranging said acknowledges based on predetermined characteristics.

8. A switch having *n* non-blocking paths, said switch comprising a circuit as claimed in claim 1.

9. A multiple arbitration circuit capable of simultaneously arbitrating multiple paths from at least one source port to at least one destination port through a switch comprising: a crosspoint switch and a multiple arbitration unit, said multiple arbitration unit comprising a

request decoder, a prioritizer, a crosspoint select encoder and an acknowledge OR, wherein if a source port is requesting a destination port that no other source port is requesting, then said requested destination port can be arbitrated simultaneously with requests by source ports for other destination ports.

10. A circuit according to claim 9, wherein said switch is a 32 port switch, and 32 ports can arbitrate for 32 separate destinations in a single arbitration cycle of said circuit.

11. A storage area network comprising a director switch with a circuit as claimed in claim 9.

12. A method for making a director switch comprising the steps of obtaining a circuit as claimed in claim 1 and implementing said circuit in said director switch for the purpose of arbitrating datapaths therethrough.

13. A method for making a circuit usable in a switch having multiple source ports and multiple destination ports comprising the steps of: configuring a field programmable gate array such that when a source port is requesting a destination port that no other source port is requesting, then said destination port can be arbitrated simultaneously with requests by other source ports for other destination ports.

14. A method interconnecting processors and/or peripherals through a switch employing a multiple arbitration circuit having a crosspoint switched bus, said method comprising the steps of:

simultaneously arbitrating multiple paths from *n* source ports associated with said processors or said peripherals to *n* destination ports associated with said processors or peripherals at the same instance in time, wherein *n* represents the maximum number of ports on said crosspoint switched bus through said multiple arbitration circuit;

connecting at least one of said *n* destination ports to at least one of said *n* source ports.